WHAT IS CLAIMED IS:

1. A semiconductor device having a multiple layer wiring structure that is provided with two or more metal layers and having a stack VIA portion in which, when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more intermediate metal layers, the intermediate metal layers are connected in sequence starting from the intermediate metal layer adjacent to the connection metal layer, wherein

the semiconductor device having a multiple layer wiring structure is provided with:

two or more partitioned intermediate metal layers that are partitioned the intermediate metal layer inside the connection area; and

an intermediate metal layer wiring area that is sandwiched by the partitioned intermediate metal layers.

2. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the connection area is an intersection portion where the connection metal layer and the layer to be connected intersect.

3. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the intermediate metal layer wiring area is formed in a priority wiring direction in the intermediate metal layer.

4. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein appropriate partitioned areas of the intermediate metal layers are secured and the intermediate metal layer wiring areas are formed by deleting appropriate interlayer connection portions that connect the

metal layers forming the stack VIA portion.

5. The semiconductor device having a multiple layer wiring structure according to claim 4, wherein the interlayer connection portions are arranged in an array configuration that matches wiring tracks running in the priority wiring direction in the intermediate metal layers connected to the interlayer connection portions, and are deleted where appropriate in row units running in the priority wiring direction.

6. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the partitioned intermediate metal layers are formed in accordance with minimum design rules in a transverse direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

7. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the layer to be connected is a metal layer.

8. The semiconductor device having a multiple layer wiring structure according to claim 1, wherein the layer to be connected is a non-metal layer.

9. The semiconductor device having a multiple layer wiring structure according to claim 8, wherein the non-metal layer is a polycrystalline silicon layer.

10. The semiconductor device having a multiple layer wiring structure according to claim 8, wherein the non-metal layer is a diffusion layer.

11. A wiring method for a semiconductor device having a multiple layer wiring structure for two or more metal layers and a stack VIA portion in which, when connecting in a connection area a connection metal layer and a layer to be connected that is removed from the connection metal layer with one or more

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intermediate metal layers, the intermediate metal layers are connected in sequence starting from the intermediate metal layer adjacent to the connection metal layer, wherein

the intermediate metal layers are partitioned within the connection area, and an area sandwiched by the partitioned intermediate metal layers is formed as an intermediate metal layer wiring area.

12. The wiring method for a semiconductor device having a multiple layer wiring structure according to claim 11, wherein the connection area is formed at an intersection portion where the connection metal layer and the layer to be connected intersect.

13. The wiring method for a semiconductor device having a multiple layer wiring structure according to claim 11, wherein the intermediate metal layer wiring area is formed in the priority wiring direction in the intermediate metal layer.

14. The wiring method for a semiconductor device having a multiple layer wiring structure according to claim 11, wherein appropriate partitioned areas of the intermediate metal layers are secured and the intermediate metal layer wiring areas are formed by deleting appropriate interlayer connection portions that connect the metal layers forming the stack VIA portion.

15. The wiring method for a semiconductor device having a multiple layer wiring structure according to claim 14, wherein the interlayer connection portions are arranged in an array configuration that matches wiring tracks running in the priority wiring direction in the intermediate metal layers connected to the interlayer connection portions, and are deleted where appropriate in row units running in the priority wiring direction.

16. The wiring method for a semiconductor device having a multiple layer wiring structure according to claim 11, wherein the partitioned intermediate metal layers are formed in accordance with minimum design rules in a transverse direction that is orthogonal to the priority wiring direction of the intermediate metal layer.

17. A wiring device for a semiconductor device having a multiple layer wiring structure, wherein the wiring device is provided with an automatic wiring design program for performing wiring design automatically using the wiring method for a semiconductor device having a multiple layer wiring structure described in claim 11.

18. A recording medium on which is recorded an automatic wiring design program for performing wiring design automatically using the wiring method for a semiconductor device having a multiple layer wiring structure described in claim 11.